

CLAIMS

What is claimed is:

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1. A modified glitch latch, said modified glitch latch comprising:

a modified glitch latch output terminal;

a control circuit, said control circuit comprising
10 a control circuit first input terminal, a control circuit second input terminal and a control circuit output terminal;

a clock signal coupled to said control circuit first input terminal, said clock signal having a first
15 or "A" phase and a second or "B" phase;

a read signal coupled to said control circuit second input terminal, said read signal having a first or inactive phase and a second or active phase,
wherein;

20 a control signal from said control circuit output terminal opens said modified glitch latch only when, both:

said clock signal is in said "B" phase; and

said read signal is in said active phase.

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2. The structure of Claim 1, wherein;

said modified glitch latch is a sensing element coupled to a read word line of a retirement payload

array and said second or active phase of said read signal corresponds to a shift in position of a read pointer of said retirement payload array.

5 3. The method of Claim 2, wherein;
 said retirement payload array comprises M read word lines and N read bit lines, further wherein;
 each of said M read word lines is coupled to a corresponding one of M modified glitch latches.

10 4. The method of Claim 3, wherein;
 said number of rows M is equal to 16 and said number of columns N is equal to 192 such that said retirement payload array is a 192 column and 16 row
15 retirement payload array.

 5. The method of Claim 3, wherein;
 said retirement payload array is a 192 column, 16-
read word line register file structure employing a
20 dynamic, full swing pull down read mechanism.

 6. A modified glitch latch, said modified glitch latch comprising:
25 a modified glitch latch first input terminal;
 a signal IN coupled to said modified glitch latch first input terminal;

a first inverter, said first inverter comprising
a first inverter input terminal coupled to said
modified glitch latch first input terminal and a first
inverter output terminal;

5 an OR gate, said OR gate comprising an OR gate
first input terminal, an OR gate second input terminal,
coupled to said first inverter output terminal, and an
OR gate output terminal;

10 a first NAND gate, said first NAND gate comprising
a first NAND gate first input terminal, coupled to said
OR gate output terminal, a first NAND gate second input
terminal and a first NAND gate output terminal;

15 a NOR gate, said NOR gate comprising a NOR gate
first input terminal, coupled to said NAND gate output
terminal, a NOR gate second input terminal, coupled to
said modified glitch latch first input terminal and a
NOR gate output terminal, coupled to said a first NAND
gate second input terminal;

20 a modified glitch latch output terminal coupled to
said NOR gate output terminal;

a control circuit, said control circuit comprising
a control circuit first input terminal, a control
circuit second input terminal and a control circuit
output terminal;

25 a clock signal coupled to said control circuit
first input terminal, said clock signal having a first
or "A" phase and a second or "B" phase;

an read signal coupled to said control circuit second input terminal, said read signal having a first or inactive phase and a second or active phase, wherein;

5 said control circuit output terminal is coupled to said OR gate first input terminal such that a control signal from said control circuit output terminal is coupled to said OR gate first input terminal, further wherein:

10 said control signal from said control circuit output terminal opens said modified glitch latch only when, both:

 said clock signal is in said "B" phase; and
 said read signal is in said active phase.

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7. The structure of Claim 6, wherein;

 said modified glitch latch is a sensing element coupled to a read word line of a retirement payload array and said second or active phase of said read
20 signal corresponds to a shift in position of a read pointer of said retirement payload array.

8. The method of Claim 7, wherein;

 said retirement payload array comprises M read
25 word lines and N read bit lines, further wherein;

 each of said M read word lines is coupled to a corresponding one of M modified glitch latches.

9. The method of Claim 8, wherein;

said number of rows M is equal to 16 and said
number of columns N is equal to 192 such that said
retirement payload array is a 192 column and 16 row
5 retirement payload array.

10. The method of Claim 8, wherein;

said retirement payload array is a 192 column, 16-
read word line register file structure employing a
10 dynamic, full swing pull down read mechanism.

11. The modified glitch latch of Claim 6,
wherein;

15 said control circuit comprises:

a second inverter, said second inverter comprising
a second inverter input terminal, coupled to said
control circuit first input terminal, and a second
inverter output terminal;

20 a second NAND gate, said second NAND gate
comprising a second NAND gate first input terminal,
coupled to said control circuit second input terminal,
a second NAND gate second input terminal, coupled to
said second inverter output terminal, and a second NAND
25 gate output terminal coupled to said control circuit
output terminal.

12. The structure of Claim 11, wherein;

said modified glitch latch is a sensing element coupled to a read word line of a retirement payload array.

5 13. The method of Claim 12, wherein;
 said retirement payload array comprises M read word lines and N read bit lines, further wherein;
 each of said M read word lines is coupled to a corresponding one of M modified glitch latches.

10 14. The method of Claim 13, wherein;
 said number of rows M is equal to 16 and said number of columns N is equal to 192 such that said retirement payload array is a 192 column and 16 row
15 retirement payload array.

 15. The method of Claim 13, wherein;
 said retirement payload array is a 192 column, 16-read word line register file structure employing a
20 dynamic, full swing pull down read mechanism.

 16. A method for controlling the operation of a modified glitch latch, said method comprising:
 receiving a clock signal, said clock signal having
25 a first or "A" phase and a second or "B" phase;
 receiving a read signal, said read signal having a first or inactive phase and a second or active phase;
 and

opening said modified glitch latch only when,
both:

said clock signal is in said "B" phase;
and said read signal is in said active phase.

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17. The method of Claim 16, wherein;

said glitch latch is a sensing element coupled to
a read word line of a retirement payload array and said
second or active phase of said read signal corresponds
10 to a shift in position of a read pointer of said
retirement payload array.

18. The method of Claim 17, wherein;

said retirement payload array comprises M read
15 word lines and N read bit lines, further wherein;
each of said M read word lines is coupled to a
corresponding one of M modified glitch latches.

19. The method of Claim 18, wherein;

20 said number of rows M is equal to 16 and said
number of columns N is equal to 192 such that said
retirement payload array is a 192 column and 16 row
retirement payload array.

25 20. The method of Claim 19, wherein;

said retirement payload array is a 192 column, 16-
read word line register file structure employing a
dynamic, full swing pull down read mechanism.

21. A method for performing conditional reads of a retirement payload array in a microprocessor, said method comprising:

5 providing a retirement payload array, said retirement payload array comprising M rows of memory cells and N columns of memory cells; said retirement payload array further comprising M read word lines and N read bit lines, wherein, each of said N read bit
10 lines is coupled to a corresponding pre-charge device and a corresponding sensing device;

coupling a clock signal to said retirement payload array, said clock signal having a first or "A" phase and a second or "B" phase; wherein said pre-charge
15 devices are pre-charged when said clock signal is in said first or "A" phase;

coupling a read signal to said retirement payload array, said read signal having a first or inactive phase and a second or active phase, said second or
20 active phase of said read signal corresponding to a shift in position of a read pointer of said retirement payload array;

initiating a read of said retirement payload array only when, both:

25 said clock signal is in said "B" phase; and
said read signal is in said active phase;

coupling M modified glitch latches, one each, to each of said M read word lines;

coupling said clock signal to a first input
terminal of each of said M modified glitch latches;

coupling said read signal to a second input
terminal of each of said M modified glitch latches;

5 opening said modified glitch latch only when,
both:

said clock signal is in said "B" phase; and

said read signal is in said active phase.

10 22. The method of Claim 21, wherein;

said number of rows M is equal to 16 and said
number of columns N is equal to 192 such that said
retirement payload array is a 192 column and 16 row
retirement payload array.

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23. The method of Claim 22, wherein;

said retirement payload array is a 192 column, 16-
read word line register file structure employing a
20 dynamic, full swing pull down read mechanism.